AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): An electrostatic discharge (ESD) protection circuit electrically connected to an input/output (I/O) buffering pad, an internal circuit, a [[V_{SS}]]Vss power terminal, and a [[V_{DD}]]Vdd power terminal, the ESD protection circuit comprising:

a first ESD-detection circuit electrically connected between the I/O buffering pad and the [[V_{SS}]]Vss power terminal;

a P-type substrate-triggered silicon controlled rectifier (P-STSCR) comprising a first lateral silicon controlled rectifier (SCR) and a P-type trigger node, an anode and a cathode of the P-STSCR being electrically connected to the I/O buffering pad and the [[V_{SS}]]Vss power terminal respectively;

a second ESD-detection circuit electrically connected between the I/O buffering pad and the [[V_{DD}]]Vdd power terminal; and

an N-type substrate-triggered silicon controlled rectifier (N-STSCR) comprising a second lateral SCR and an N-type trigger node, a cathode and an anode of the N-STSCR being electrically connected to the I/O buffering pad and the [[V_{DD}]]Vdd power terminal respectively.

Claim 2 (original): The ESD protection circuit of claim 1 wherein the P-STSCR further comprises:

a P-type substrate;

an N-well in the P-type substrate;

a first N^+ diffusion region and a first P^+ diffusion

region in P-type substrate for use as the cathode of the P-STSCR; and

a second N^+ diffusion region and a second P^+ diffusion region in the N-well for use as the anode of the P-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the first lateral SCR.

Claim 3 (currently amended): The ESD protection circuit of claim 2 wherein when a positive voltage pulse is applied to the I/O buffering pad, the first ESD detection circuit produces a first trigger current flowing into the P-type trigger node of the P-STSCR to trigger the first lateral SCR in the P-STSCR to enter a latch state, the latch state quickly turning on the P-STSCR so that a current incurred from the positive voltage pulse is discharged to the [[V_{SS}]]Vss power terminal.

Claim 4 (original): The ESD protection circuit of claim 1 wherein the N-STSCR in the ESD protection circuit further comprises:

a P-type substrate;

an N-well in the P-type substrate;

a first N^+ diffusion region and a first P^+ diffusion region in P-type substrate for use as the cathode of the N-STSCR; and

a second N^+ diffusion region and a second P^+ diffusion region in the N-well for use as the anode of the N-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the second lateral SCR.

Claim 5 (currently amended): The ESD protection circuit of claim 4 wherein when a negative voltage pulse is applied to the I/O buffering pad, the second ESD detection circuit produces a second trigger current that flows into the N-type trigger node of the N-STSCR to trigger the second lateral SCR in the N-STSCR to enter a latch state, the latch state quickly turning on the N-STSCR so that current incurred from the negative voltage pulse is discharged to the [[V_{DD}]]Vdd power terminal.

Claim 6 (currently amended): The ESD protection circuit of claim 1 wherein the first ESD ~~protection~~detection circuit comprises a first resistor, a first capacitor, a zener diode, a diode string or an NMOS.

Claim 7 (original): The ESD protection circuit of claim 6 wherein the NMOS enhances the first trigger current so as to accelerate the triggering of the P-STSCR.

Claim 8 (original): The ESD protection circuit of claim 1 wherein the second ESD detection circuit comprises a second resistor, a second capacitor, a zener diode, a diode string or a PMOS.

Claim 9 (original): The ESD protection circuit of claim 8 wherein the PMOS enhances the second trigger current so as to accelerate the triggering of the N-STSCR.

Claim 10 (currently amended): The ESD protection

circuit of claim 1 wherein the fist ESD detection circuit comprises a third resistor, a third capacitor and a first inverter, an input node of the first inverter electrically connected to the [[V_{DD}]]Vdd power terminal and the [[V_{SS}]]Vss power terminal through the third resistor and the third capacitor respectively, an output node of the first inverter electrically connected to the P-type trigger node of the P-STSCR.

Claim 11 (currently amended): The ESD protection circuit of claim 10 wherein when a positive ESD voltage pulse is applied to the I/O buffering pad, the first inverter is charged by the positive ESD voltage pulse to generate a third trigger current at the output node of the first inverter, the third trigger current flowing into the P-type trigger node of the P-STSCR to trigger the fist lateral SCR, the first lateral SCR entering a latch state in response to the third trigger current and quickly turning on the P-STSCR so that current incurred from the positive voltage pulse is discharged to the [[V_{SS}]]Vss power terminal.

Claim 12 (currently amended): The ESD protection circuit of claim 1 wherein the second ESD detection circuit comprises a fourth resistor, a fourth capacitor, and a second inverter, an input node of the second inverter electrically connected to the [[V_{SS}]]Vss power terminal and the [[V_{DD}]]Vdd power terminal through the fourth resistor and the fourth capacitor respectively, an output node of the second inverter electrically connected to the N-type trigger

node of the N-STSCR.

Claim 13 (currently amended): The ESD protection circuit of claim 12 wherein when a negative ESD voltage pulse is applied to the I/O buffering pad, the output node of the second inverter is charged by the negative ESD voltage pulse to generate a fourth trigger current at the N-type trigger node of the N-STSCR to trigger the second lateral SCR, the second lateral SCR entering a latch state in response to the fourth trigger current to turn on the N-STSCR quickly so that current incurred from the negative voltage pulse is discharged to the [[V_{DD}]]Vdd power terminal.

Claim 14 (currently amended): An electrostatic discharge (ESD) protection circuit electrically connected to an I/O buffering pad, an internal circuit, a [[V_{SS}]]Vss power terminal and a [[V_{DD}]]Vdd power terminal, the ESD protection circuit comprising:

a first ESD-detection circuit electrically connected between the I/O buffering pad and the [[V_{SS}]]Vss power terminal;

a first stacked silicon controlled rectifier (SCR) electrically connected between the [[V_{SS}]]Vss power terminal and the I/O buffering pad, the first stacked SCR series connected by a plurality of P-type substrate-triggered silicon controlled rectifiers (P-STSCR), each P-STSCR comprising a first lateral SCR and a P-type trigger node;

a second ESD-detection circuit electrically connected between the I/O buffering pad and the [[V_{DD}]]Vdd power terminal; and

a second stacked SCR electrically connected between the [[V_{DD}]]Vdd power terminal and the I/O buffering pad, the second stacked SCR series connected by a plurality of N-type substrate-triggered silicon controlled rectifiers (N-STSCR), each N-STSCR comprising a second lateral SCR and an N-type trigger node;

wherein a total holding voltage for the first stacked SCR is greater than a maximum voltage level of a normal signal on the I/O buffering pad, and a total holding voltage for the second stacked SCR is less than a minimum voltage level of the normal signal on the I/O buffering pad, so as to prevent normal signals from being interfered because of the unexpected turn-on of the ESD protection circuit by noise.

Claim 15 (original): The ESD protection circuit of claim 14 wherein each P-STSCR further comprises:

a P-type substrate;

an N-well in the P-type substrate;

a first N^+ diffusion region and a first P^+ diffusion region in the P-type substrate for use as the cathode of the P-STSCR; and

a second N^+ diffusion region and a second P^+ diffusion region in the N-well for use as the anode of the P-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the first lateral SCR.

Claim 16 (original): The ESD protection circuit of claim 14 wherein the first stacked SCR further comprises a plurality of diodes series connected with each P-STSCR.

Claim 17 (original): The ESD protection circuit of claim 14 wherein each N-STSCR further comprises:

a P-type substrate;

an N-well in the P-type substrate;

a first N^+ diffusion region and a first P^+ diffusion region in the P-type substrate for use as the cathode of the N-STSCR; and

a second N^+ diffusion region and a second P^+ diffusion region in the N-well for use as the anode of the N-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the second lateral SCR.

Claim 18 (original): The ESD protection circuit of claim 14 wherein the second stacked SCR further comprises a plurality of diodes series connected with each N-STSCR.

Claim 19-33 (canceled)

Claim 34 (currently amended): A power-rail ESD clamp circuit for use with mixed voltages, the power-rail ESD clamp circuit being electrically connected between a [[V_{SS}]]Vss power terminal and a [[V_{DD}]]Vdd power terminal comprising a first Vdd power terminal and a second Vdd power terminal, the power-rail ESD clamp circuit comprising ~~a plurality of sub power-rail ESD clamp circuits~~ a first sub power-rail ESD clamp circuit, a second sub power-rail ESD clamp circuit and a third sub power-rail ESD clamp circuit, each of the sub power-rail ESD clamp circuits comprises:

an ESD-detection circuit; and

at least one substrate-triggered silicon controlled rectifier (STSCR), the STSCR comprising a lateral silicon controlled rectifier (SCR) and at least one trigger node;

wherein the first sub power-rail ESD clamp circuit is electrically connected between the first Vdd power terminal and the Vss power terminal; the second sub power-rail ESD clamp circuit is electrically connected between the first Vdd power terminal and the second Vdd power terminal; and the third sub power-rail ESD clamp circuit is electrically connected between the second Vdd power terminal and the Vss power terminal.

Claim 35 (canceled)

Claim 36 (currently amended): The power-rail ESD clamp circuit of claim [[35]]34 wherein the STSCR is a P-type substrate-triggered silicon controlled rectifier (P-STSCR) and the trigger node is a P-type trigger node.

Claim 37 (currently amended): The power-rail ESD clamp circuit of claim [[35]]34 wherein the substrate-triggered silicon controlled rectifier is an N-type substrate-triggered silicon controlled rectifier (N-STSCR) and the trigger node is an N-type trigger node.

Claim 38 (currently amended): The power-rail ESD clamp circuit of claim [[35]]34 wherein the substrate-triggered silicon controlled rectifier

(STSCR) is a double-triggered silicon controlled rectifier (DT-SCR) and the DT-SCR comprises a P-type trigger node and an N-type trigger node.

Claim 39 (currently amended): The power-rail ESD clamp circuit of claim [[35]]34 wherein a plurality of diodes are series connected with the STSCR.

Claim 40-43 (canceled)

Claim 44 (currently amended): An ESD-connection circuit for use in separated power rails, the separated power rails comprising a first [[V_{SS}]]Vss power terminal, a first [[V_{DD}]]Vdd power terminal, a second [[V_{SS}]]Vss power terminal, and a second [[V_{DD}]]Vdd power terminal, a first core circuit connected between the first [[V_{DD}]]Vdd power terminal and the first [[V_{SS}]]Vss power terminal, a second core circuit connected between the second [[V_{DD}]]Vdd power terminal and the second [[V_{SS}]]Vss power terminal, the ESD-connection circuit comprising:

at least one ESD-detection circuit;

a first sub ESD-connection circuit directly connected between the first Vdd power terminal and the second Vdd power terminal;

a second sub ESD-connection circuit directly connected between the first Vdd power terminal and the second Vdd power terminal;

a third sub ESD-connection circuit directly connected between the first Vss power terminal and the second Vss power terminal; and

a fourth sub ESD-connection circuit directly

connected between the first Vss power terminal and the second Vss power terminal.

Claim 45 (original): The ESD-connection circuit of claim 44 wherein each of the sub ESD-connection circuits further comprises at least one substrate-triggered silicon controlled rectifier (STSCR), the STSCR comprising a lateral silicon controlled rectifier (SCR) and at least one trigger node.

Claim 46 (original): The ESD-connection circuit of claim 45 wherein the STSCR is a P-type substrate-triggered silicon controlled rectifier (P-STSCR) and the trigger node is a P-type trigger node.

Claim 47 (original): The ESD-connection circuit of claim 45 wherein the substrate-triggered silicon controlled rectifier is an N-type substrate-triggered silicon controlled rectifier (N-STSCR) and the trigger node is an N-type trigger node.

Claim 48 (original): The ESD-connection circuit of claim 45 wherein the substrate-triggered silicon controlled rectifier (STSCR) is a double-triggered silicon controlled rectifier (DT-SCR) and the DT-SCR comprises a P-type trigger node and an N-type trigger node.

Claim 49 (original): The ESD-connection circuit of claim 45 wherein a plurality of diodes are series

connected with the STSCR.

Claim 50 (currently amended): The ESD-connection circuit of claim 45 wherein an anode, a cathode and each trigger node of the first sub ESD-connection circuit are electrically connected to the first [[V_{DD}]]Vdd power terminal, the second [[V_{DD}]]Vdd power terminal, and the ESD detection circuit, respectively.

Claim 51 (currently amended): The ESD-connection circuit of claim 45 wherein an anode, a cathode and each trigger node of the second sub ESD-connection circuit are electrically connected to the second [[V_{DD}]]Vdd power terminal, the first [[V_{DD}]]Vdd power terminal, and the ESD detection circuit, respectively.

Claim 52 (currently amended): The ESD-connection circuit of claim 45 wherein an anode, a cathode and each trigger node of the third sub ESD-connection circuit are electrically connected to the second [[V_{SS}]]Vss power terminal, the first [[V_{SS}]]Vss power terminal, and the ESD detection circuit, respectively.

Claim 53 (currently amended): The ESD-connection circuit of claim 45 wherein an anode, a cathode and each trigger node of the fourth sub ESD-connection circuit are electrically connected to the first [[V_{SS}]]Vss power terminal, the second [[V_{SS}]]Vss power terminal, and the ESD detection circuit, respectively.

Claim 54 (currently amended): The ESD-connection circuit of claim 44 wherein the ESD-detection circuit

is electrically connected between the first [[V_{DD}]]Vdd power terminal and the first [[V_{SS}]]Vss power terminal.

Claim 55 (currently amended): The ESD-connection circuit of claim 44 wherein the ESD-detection circuit is electrically connected between the second [[V_{DD}]]Vdd power terminal and the second [[V_{SS}]]Vss power terminal.